VIGNAN'S
Foundation for Science, Technology & Research
(Deemed to be UNIVERSITY)
-Estd. u/s 3 of UGC Act 1956

DEPARTMENT OF ELECTRONICS AND COMMUNCATION ENGINEERING

18-07-2020

Minutes of the Board of studies (BOS) meeting for MTech VLSI(VT) held on18.07.2020in SRUJANA Seminar hall.

The following External members attended for the BOS meeting on 18-07-2020

1. Dr.P.Srihari Rao, Professor, Dept. of ECE, NIT Warangal.
2. Dr. K.Subbarangaiah, Director, VEDA IIT, Hyderabad.
3. Mr. B.Kalyan Chakravarthi, Technical Director, Eleego Circuits Pvt.Ltd., Bangalore..
4. Dr.B. Subramanyam, Analog Design Engineer, Intel, Bangalore.
5. Mr.Damodara M.S, Entuple Technologies, Hyderabad

The BOS meeting for MTech (VLSI Design) Programme was held on 18-07-2020 in COE though ZOOM from 10:00AM to 01:15PM. HOD Sir Welcomed the all the BOS Members and initiated the meeting with briefing of agenda. All the BOS members appreciated our structure and given their valuable suggestions.

- Following are the recommendations given by BOS Members:
  - Dr P Srihari agreed our proposed structure and appreciated that the proposed curriculum has covered all the different areas of industry and Research. And he has given good inputs for all the courses.
  - Dr.Subbarangaih Suggested that Programming languages/Scripting Languages should be included in core subjects instead of electives. He suggested to standardise thequestion paper with more design problems.
  - He advised to increase the number of assignments.
  - In the third semester instead of only MOOCS course, he suggested **MOOCS/INDUSTRY Course.**
  - Dr.Subhramanyam accepted our proposed structure as it is and appreciated the Curriculum. and he said that it is helpful for more placement if ASIC is taught by industry persons and he suggested good textbooks for different courses.

- Mr. Damodara suggested that ASIC Design course need to be industry oriented as more opportunities are available in this field.
- AICD and DICD are purely CMOS, so he suggested to merge both courses to shift ASIC design course from electives to core. And, he suggested to strengthen FPGA Course. He advised to have FPGA course and System Design Course separately.
- Mr Kalyan also accepted our proposed structure as it is and suggested to integrate all the mini projects to get system level project.
- He suggested to include Bipolar Designs in related courses.
- Logical Design suggested to be included in the DICD Subject.
- Instead of only Python, they suggested to include TCL/TK in scripting languages.
- They suggested to remove unit 2 -Testing from ADSD Course as it is covered in VLSI testing course.
- They suggested to use lab with Python for the Physical Design Automation Course.
- They suggested to elaborate RFIC Design course and advised to have practical's/mini projects to make it design oriented.
- They suggested to add System Verilog and UVM verification in verification methodologies course with C++ as Unit 1.
- They suggested have Micro/Nano Fluidic course as a MOOCS course.
- They advised to change the title of PUF to Hardware Security.
- They suggested to modify Biomedical Electronics subject as VLSI Circuits for Biomedical Applications.

VIGNAN'S
Foundation for Science, Technology & Research
(Deemed to be UNIVERSITY)
-Estd. u/s 3 of UGC Act 1956

BOS OUTCOMES :

1. BOS members approved the revised curriculum (Structure, Syllabus and regulations) of MTech VLSI and it follows Choice Based Credit System . Course Structure is provided in Appendix I.
2. Major restructuring has taken place in the Curriculum with theory courses integrated with laboratory sessions.
3. All the Courses in the Curriculum are designed to fall under either of the domains of employability (or) skill development (or) Entrepreneurship. The mapping of the courses with employability or skill development is provided in Appendix II.
4. In all the courses of the revised curriculum (R20) substantial changes are made in the content. The percentage of revision from R17 – R20 is 25%.
5. Stakeholders feedback is collected, analysed, and given utmost priority while designing the curriculum and their suggestions are implemented.
6. The finalized Course Structure is shown in Appendix II and III

VIGNAN'S
Foundation for Science, Technology & Research
(Deemed to be University)
Estd. u/s 3 of UGC Act 1956

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Appendix-I

Course Structure

M.Tech VLSI Design

Semester - I

Course Title	Proposed Course	L	T	P	C
Core course- 1	Analog IC Design	3	-	2	4
Core Course- 2	Digital IC Design	3	-	2	4
Core Course- 3	Semiconductor Device Modelling	3	-	-	3
Core Course- 4	FPGA Based system Design	3	-	2	4
Dept Elective - 1		3	-	-	3
Audit course - 1		1	-	-	-
Minor Project		-	-	3	2
Credits					**20**

Semester - II

Course Title	Proposed Course	L	T	P	C
Core course- 5	Mixed Signal Design	3	-	2	4
Core Course- 6	VLSI Testing & Validation	3	-	-	3
Dept Elective -2		3	-	-	3
Dept Elective -3		3	-	-	3
Research methodology & IPR		2	-	-	2
Audit course-2		1	-	-	-

EOP		-	-	3	2
Societal centric / Industry Oriented Project		-	-	3	2
	Credits				**19**

L=Lecture Hours; T=Tutorial Hours; P=Practical Hours;

Semester - III

Course Title	**L**	**T**	**P**	**C**
MOOCS Course-1	3	-	-	3
MOOCS Course-2	3	-	-	3
		Total		6

Semester - IV

Course Title	**L**	**T**	**P**	**C**
Project / Internship Phase-1	-	-	20	10
Project / Internship Phase-2	-	-	32	16
				26

Total Credits – 71

Elective Courses

S.no	Subject name
1	MICROCHIP FABRICATION TECHNOLOGY
2	PYTHON/TCL FOR SOFTWARE HARDWARE CO-DESIGN
3	ADVANCED DIGITAL SYSTEM DESIGN
4	VLSI SIGNAL PROCESSING
5	LOW POWER VLSI DESIGN
6	PHYSICAL DESIGN AUTOMATION
7	CMOS RF INTEGRATED CIRCUITS
9	ASIC DESIGN
10	SENSORS AND SENSOR CIRCUIT DESIGN
11	VERIFICATION METHODOLOGIES
12	SOC DESIGN
13	MEMORY DESIGN AND TESTING
14	MEMS & NEMS
15	POWER MANAGEMENT CIRCUITS
16	NANO OPTICS
17	NANO ELECTRONIC DEVICES
18	MICRO NANO FLUIDICS
19	HARDWARE SECURITY
20	VLSI CIRCUITS FOR BIOMEDICAL APPLICATIONS

Note: The courses that are highlighted denotes implementation of " Choice Based Credit System (CBCS)"

Audit course 1 & 2

(Reference from AICTE Model Curriculum 2018)

S.NO	SUBJECT
1	Technical Report Writing
2	Sanskrit for Technical Knowledge
3	Constitution of India
4	Value Education
5	Pedagogy Studies
6	Stress Management by YOGA
7	Disaster Management
8	Personality Development through Life Enlightenment Skills

Note: The courses that are highlighted denotes implementation of "Choice Based Credit System(CBCS)"

Signature of BOS chairman

APPENDIX – II

List of courses that enable employability or entrepreneurship or skill development in the R-20 MTech – VLSI

Sl.	Course Name	Core / Elective	Year	Employability / Skill Development/Entrepreneurship
1	Analog IC Design	Core	I	Skill Development
2	Digital IC Design	Core	I	Skill Development
3	VLSI Technology	Core	I	Skill Development
4	Semiconductor Device Modeling	Core	I	Employability
5	Mixed Signal Design	Core	I	Skill Development
6	VLSI Testing and Validation	Core	I	Employability
7	**Low power VLSI Design**	Elective	I	Skill Development
8	**MICROCHIP FABRICATION TECHNOLOGY**	Elective	I	Skill Development
9	**PYTHON/TCL FOR SOFTWARE HARDWARE CO-DESIGN**	Elective	I	Skill Development
10	**ADVANCED DIGITAL SYSTEM DESIGN**	Elective	I	Skill Development
11	**VLSI SIGNAL PROCESSING**	Elective	I	Skill Development
12	**PHYSICAL DESIGN AUTOMATION**	Elective	I	Employability
13	**CMOS RF INTEGRATED CIRCUITS**	Elective	I	Skill Development

14	**ASIC DESIGN**	Elective	I	Skill Development
15	**SENSORS AND SENSOR CIRCUIT DESIGN**	Elective	I	Skill Development
16	**VERIFICATION METHODOLOGIES**	Elective	I	Skill Development
17	**SOC DESIGN**	Elective	I	Skill Development
18	**MEMORY DESIGN AND TESTING**	Elective	I	Skill Development
19	**MEMS & NEMS**	Elective	I	Skill Development
20	**POWER MANAGEMENT CIRCUITS**	Elective	I	Skill Development
21	**NANO OPTICS**	Elective	I	Skill Development
22	**NANO ELECTRONIC DEVICES**	Elective	I	Skill Development
23	**MICRO NANO FLUIDICS**	Elective	I	Skill Development
24	**HARDWARE SECURITY**	Elective	I	Skill Development
25	**VLSI CIRCUITS FOR BIOMEDICAL APPLICATIONS**	Elective	I	Skill Development

Note : The courses that are highlighted denotes implementation of "Choice Based Credit System(CBCS)

Signature of BOS Chairman

APPENDIX - III

List of new courses in the R-20 Regulations

MTech – VLSI

Sl.	Course Name	Year
1	Analog IC Design	I
2	Digital IC Design	I
3	VLSI Technology	I
4	Semiconductor Device Modeling	I
5	Mixed Signal Design	I
6	VLSI Testing and Validation	I
7	**Low power VLSI Design**	I
8	**MICROCHIP FABRICATION TECHNOLOGY**	I
9	**PYTHON/TCL FOR SOFTWARE HARDWARE CO-DESIGN**	I
10	**ADVANCED DIGITAL SYSTEM DESIGN**	I
11	**VLSI SIGNAL PROCESSING**	I
12	**PHYSICAL DESIGN AUTOMATION**	I
13	**CMOS RF INTEGRATED CIRCUITS**	I
14	**ASIC DESIGN**	I
15	**SENSORS AND SENSOR CIRCUIT DESIGN**	I
16	**VERIFICATION METHODOLOGIES**	I
17	**SOC DESIGN**	I
18	**MEMORY DESIGN AND TESTING**	I
19	**MEMS & NEMS**	I
20	**POWER MANAGEMENT CIRCUITS**	I
21	**NANO OPTICS**	I
22	**NANO ELECTRONIC DEVICES**	I
23	**MICRO NANO FLUIDICS**	I

24	HARDWARE SECURITY	I
25	VLSI CIRCUITS FOR BIOMEDICAL APPLICATIONS	I

Note : The Courses that are highlighted denotes implementation of "Choice Based Credit System(CBCS)"

Signature of BOS Chairman

The following are the members present for the board of studies meeting held at Department of Electronics &Communication Engineering on 18-07-2020

External Members :

Sl. No.	Name of the Member	Designation	Signature
1.	Dr.P.Srihari Rao	Professor, Dept. of ECE, NIT Warangal	
2.	Dr. K.Subbarangaiah	Director, VEDA IIT, Hyderabad	
3	Mr. B.KalyanChakravarthi	Technical Director, Eleego Circuits Pvt.Ltd., Bangalore.	
4	Dr.B. Subramanyam	Analog Design Engineer, Intel, Bangalore	
5	Mr.DamodaraM.S	Entuple Technologies, Hyderabad	

Internal Members :

Sl. No.	Name of the Member	Designation	Signature
1.	Dr.B.Seetharamananjaneyalu	Professor	
2.	Dr.N.Usha Rani	Professor	
3.	Mrs.M.Sarada	Professor	

BOS CHAIRMAN